The Synthesis Competition

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The Reactive Synthesis Problem

Synthesis of a controller for safety specifications:

\[ T = \text{spec} \times \text{partial implementation} \]
Reactive Synthesis – State of the Art

The Good: Many synthesis tools available

The Bad: Not comparable, even for tasks that most tools can solve

The Reasons:

• no standard language
• no common benchmarks
• no incentive to develop good, comparable tools
Format Based on Existing Standards

AIGER format:
• low-level, close to circuit
  \(\textbf{low entry barrier}\) for tools
• easy to \textit{extend to synthesis goals}:
  add option to make inputs controllable
• used in HWMCC
  \(\textbf{existing tool chain}\)
• can be used as \textit{both input and output format}
  \(\textbf{AIGER model checkers can verify outputs}\)
Growing Benchmark Library

• A set of simple toy benchmarks
• Converted (or about to convert) many benchmarks that have been used in literature, in multiple versions
• More benchmarks and variants are being developed
Categories:

Realizability Check (correctness + time)
Controller Synthesis (correctness + size + time)

parallel implementations will be evaluated separately
Long-Term Goals

- Measure progress of tools
- Extend standard language (liveness, partial information, quantitative properties)
- Conversion(s) from high-level language(s)
- Establish synthesis procedures as black boxes in applications
Please Participate!

• Send us benchmarks
• Enter the competition
• Use our standard language
• Let us know what you think

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